KiCad General Design Rules

While Altium designer allows you to import and export design rules (in .RUL format), KiCad uses a different approach for managing design constraints. KiCad does not currently provide a dedicated rule import/export system equivalent to that of Altium. Instead, design rules are typically managed through project template and custom design rule files.

For the ITLL PCB fabrication process, two practical methods can be used to maintain PCB rules for students using KiCad:

Method 1:
KiCad allows users to define custom rules directly within a project through:
File > Board Setup > Design Rules > Custom Rules
The rule definition can be copied and pasted into the Custom Rules text box. Once applied, these rules are stored within the project and enforced during the Design Rule Check (DRC). The full rule sets are included below in the Code portion of the Appendix.

Method 2:
A prebuilt. kicad_dru file is provided on the ITLL website (as well as below in Files section of Appendix).
Students can use this file by:
1) Downloading the .kicad_dru file
2) Copying it into their own KiCad project directory or folder
3) Renaming the file to match their exact project name
For example, if a student's project name is
"Tanner Sones PCB.kicad_pro"
Then the rule file must be renamed to and from:
"Preferred Rules.kicad_dru" to "Tanner Sones PCB.kicad_dru"
KiCad will automatically detect this file and apply these rules when the project is opened in the PCB editor.

Appendix:

Files:

Bare Minimum Rules – Bare Minimum Rules.kicad_dru

Preferred Rules – Preferred Rules.kicad_dru

Code:

Preferred Design Rules

```
(version 1)
# Preferred Manufacturing Rules
(rule "Trace Width Limits"
    (constraint track_width (min 12mil) (max 1000mil))
)
(rule "Clearance"
    (constraint clearance (min 12mil))
)
(rule "Annular Ring"
    (constraint annular_width (min 13.189mil))
)
(rule "Via Diameter"
    (constraint via_diameter (min 50mil) (max 2000mil))
)
(rule "Hole Size"
    (constraint hole_size (min 23.622mil) (max 118.11mil))
)
(rule "Copper To Hole Clearance"
    (constraint hole_clearance (min 12mil))
)
(rule "Copper To Edge Clearance"
    (constraint edge_clearance (min 12mil))
)
(rule "Hole To Hole Clearance"
    (constraint hole_to_hole (min 10mil))
)
# Differential Pair Rules
(rule "Differential Pair Gap"
    (constraint diff_pair_gap (min 12mil) (max 10mil))
)
```

Bare Minimum Design Rules

```
(version 1)
# Bare Minimum Manufacturing Rules
(rule "Trace Width Limits"
    (constraint track_width (min 4mil) (max 1000mil))
)
(rule "Clearance"
```

```
    (constraint clearance (min 4mil))
)
(rule "Annular Ring"
    (constraint annular_width (min 2mil))
)
(rule "Via Diameter"
    (constraint via_diameter (min 19.748mil) (max 2000mil))
)
(rule "Hole Size"
    (constraint hole_size (min 15.748mil) (max 118.11mil))
)
(rule "Copper To Hole Clearance"
    (constraint hole_clearance (min 4mil))
)
(rule "Copper To Edge Clearance"
    (constraint edge_clearance (min 4mil))
)
(rule "Hole To Hole Clearance"
    (constraint hole_to_hole (min 10mil))
)
# Differential Pair Rules
(rule "Differential Pair Gap"
    (constraint diff_pair_gap (min 6mil))
)
```

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